REMARKS

Claims 1-11 are pending in the application.

Claims 1-11 have been rejected.

Claims 1-11 have been amended, as set forth herein.

Claims 1-11 remain pending.

Reconsideration of the Claims is respectfully requested in light of the following remarks.

I. OBJECTION TO THE DRAWINGS

The drawings were objected to because Figures 1 and 2 have boxes without labels. However, the Applicants respectfully submit that section 608.02 Drawings of the MPEP does not require labels and states the drawings standards as follows:

V. DRAWING STANDARDS

(p) Numbers, letters, and reference characters.

(1) Reference characters (numerals are preferred), sheet numbers, and view numbers must be plain and legible, and must not be used in association with brackets or inverted commas, or enclosed within outlines, e.g., encircled. They must be oriented in the same direction as the view so as to avoid having to rotate the sheet. Reference characters should be arranged to follow the profile of the object depicted.

(2) The English alphabet must be used for letters, except where another alphabet is customarily used, such as the Greek alphabet to indicate angles, wavelengths, and mathematical formulas.

(3) Numbers, letters, and reference characters must measure at least.32 cm. (1/8 inch) in height. They should not be placed in the drawing so as to interfere with its comprehension. Therefore, they should not cross or mingle with the lines. They should not be placed upon hatched or shaded surfaces. When necessary, such as indicating a surface or cross section, a reference character may be underlined and a blank space may be left in the hatching or shading where the character occurs so that it appears distinct.

(4) The same part of an invention appearing in more than one view of the drawing must always be designated by the same reference character, and the same reference character must never be used to designate different parts.

(5) Reference characters not mentioned in the description shall not appear in the drawings. Reference characters mentioned in the description must appear in the drawings.

Thus, the Applicants elect not to add labels to the boxes of Figures 1 and 2 as labels are not required, and respectfully request withdrawal of the objection to the drawings.

II. OBJECTIONS TO THE SPECIFICATION

The abstract was objected to because the abstract should be in a separate sheet within the range of 50 to 150 words in length. By the above amendments to the specification, the Applicants have amended the abstract to be in a separate sheet within the range of 50 to 150 words in length as requested by the Examiner.

The Examiner also objected to the disclosure because the headers to identify each section are missing. By the above amendments to the specification, the Applicants have added headers to the specification to identify each section.

Accordingly, the Applicants respectfully request withdrawal of the objections to the specification.

III. CLAIM OBJECTIONS

Claims 1-11 were objected to, and the Examiner requested that references within the parentheses be removed for clarification purposes. By the above amendments to Claims 1-11, the Applicants have removed the references as requested by the Examiner and respectfully request withdrawal of the objections to Claim 1-11.

IV. REJECTION UNDER 35 U.S.C. § 101

Claims 1-11 were rejected under 35 U.S.C. § 101 as being directed to non-statutory subject matter. The rejection is respectfully traversed.

The Office Action appears to suggest that Claim 1-10 are objected to because they disclose components for composing a vector without disclosing "a practical/physical" application. However, with regard to statutory subject matter, section 706.03(a) Rejections Under 35 U.S.C. 101 [R-5] of the MPEP states:

¶ 7.05.01 Rejection, 35 U.S.C. 101, Non-Statutory
the claimed invention is directed to non-statutory subject matter because [1]
Examiner Note
In bracket 1, explain why the claimed invention is not patent eligible subject matter, e.g.,
(a) why the claimed invention does not fall within at least one of the four categories of patent eligible subject matter recited in 35 U.S.C. 101 (process, machine, manufacture, or composition of matter); or
(b) why the claimed invention is directed to a judicial exception to 35 U.S.C. 101 (i.e., an abstract idea, natural phenomenon, or law of nature) and is not directed to a practical application of such judicial exception (e.g., because the claim does not require any physical transformation and the invention as claimed does not produce a useful, concrete, and tangible result); or
(c) why the claimed invention would impermissibly cover every substantial practical application of, and thereby preempt all use of, an abstract idea, natural phenomenon, or law of nature.

The Applicants respectfully submit that the invention claimed in Claims 1-10:

1. does fall within at least one of the four categories of patent eligible subject matter recited in 35 U.S.C. 101; specifically, Claims 1-10 are directed to a machine;

2. is not directed to judicial exception to 35 U.S.C. 101, such an abstract idea, natural phenomenon, or law of nature; nonetheless, Claims 1-10 are directed to a practical application, i.e. the generation of composite-code vectors and the control of weighted sum units; and

3. does not impermissibly cover every substantial practical application of an abstract idea, natural phenomenon, or law of nature as the invention is not directed to an abstract idea, natural phenomenon, or law of nature.

Accordingly, the Applicants respectfully request withdrawal of the § 101 rejection of Claims 1-10.

The Office Action also appears to suggest that Claim 11 is objected to because Claim 11 discloses a method but fails to be directed to any specific hardware. The Applicants have amended Claim 11 to be directed to a vector processor. Accordingly, the Applicants also respectfully request withdrawal of the § 101 rejection of Claim 11.

V. REJECTION UNDER 35 U.S.C. § 102

Claims 1-11 were rejected under 35 U.S.C. § 102(e) as being anticipated by Erdogan et al. (U.S. Patent No. 7,076,514, hereinafter referred to as "Erdogan"). The rejection is respectfully traversed.

A cited prior art reference anticipates the claimed invention under 35 U.S.C. § 102 only if every element of a claimed invention is identically shown in that single reference, arranged as they are in the claims. MPEP § 2131; *In re Bond*, 910 F.2d 831, 832, 15 U.S.P.Q.2d 1566, 1567 (Fed. Cir. 1990). Anticipation is only shown where each and every limitation of the claimed invention is found in a single cited prior art reference. MPEP § 2131; *In re Donohue*, 766 F.2d 531, 534, 226 U.S.P.Q. 619, 621 (Fed. Cir. 1985).

The Applicants respectfully submit that Erdogan fails to show each and every limitation of Claim 1. Specifically, Claim 1 recites, "at least two weighted sum units, each weighted sum unit being arranged to provide an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors."

The Office Action appears to suggest that the first summer and the second summer shown in FIG. 12 of Erdogan are weighted sum units. For ease of reference, the first and second summers of Erdogan are described as follows:

> FIG. 12 illustrates a low complexity, efficient polyphase structure, according to an embodiment of the present invention. A first portion of the polyphase structure includes filters C_{11}, C_{12}, C_{13} and C_{14} for receiving inputs D_{11}, D_{12}, D_{21}, and D_{22} respectively. The outputs of filters C_{11}, C_{12}, C_{13} and C_{14} are then **combined by a first summer** and received by filter F_1. A second portion of the polyphase structure includes filters C_{21}, C_{22}, C_{23} and C_{24} for receiving inputs D_{11}, D_{12}, D_{21}, and D_{22} respectively. The outputs of filters C_{21}, C_{22}, C_{23} and C_{24} **are then combined by a second summer** and received by filter F_2. The outputs of filters F_1 and F_2 are combined by a third summer and received by a decimator structure. The decimator structure may include a Kth order integrator filter S_1, a downsampling function block N and a Kth order differentiator S_2. The decimator structure generates a digital sigma-delta output. (Col. 18, line 60-Col. 19, line 8.) (Emphasis added by the Applicants.)

Thus, the first and second summers of Erdogan simply sum the outputs of the filters and cannot be said to be **weighted** sum unit.

In distinct contrast to Erdogan, Paragraph [0009] of the Applicants' published application discloses:

> [0009] The device according to the invention is provided with at least two weighted sum units, which are able to make a selection out of a plurality of incoming basic-code vectors by means of a weighted sum operation, under the control of a configuration word. The elements of this configuration word represent the weighting factors which are used to select or deselect a basic-code vector. The selected basic-code vectors are added together and the result of the weighted sum operation is then output as an intermediate-code vector. Subsequently, the intermediate-code vectors are added together by an add unit and output as a composite-code vector. The ability to make selections out of a plurality of incoming basic-code vectors and to add intermediate-code vectors into a composite-code vector, together with the ability to configure the operations of the functional units of the device by means of configuration words, increases the flexibility of the device significantly. This flexibility is needed to support a variety of transmission standards.

Furthermore, the Office Action appears to suggest that the output of the first and second summers of Erdogan is an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors. However, the first and second summers of Erdogan relate to analog to digital conversion (ADC). They do not relate to standards and codes. For ease of reference, the sections pertaining to the filtered digital signal input and output of the first and second summers of Ergodan are set forth below:

> Another aspect of the present invention relates to Analog to Digital Conversion (ADC), which is **a process of sampling a continuous-time analog signal in time and mapping these time samples into a digital sequence with finite levels**. ADC refers to discretization of an input analog signal in both time and magnitude. For example, Sigma Delta converters provide high resolution analog to digital conversion. The high resolution may be achieved through over-sampling of an input signal at a rate higher than its bandwidth. ...
>
> An embodiment of the present invention is directed to a polyphase combiner and sigma-delta decimator block structure. ...
>
> FIG. 6 illustrates an analog to digital converter, according to an embodiment of the present invention. Analog signals are converted into digital signals by AID Converters by various methods, which may include Sigma-Delta A/D conversion. For high performance Sigma-Delta A/D conversion, an input analog signal may be sampled into a 2-bit (in some

> cases one bit or other number of bits) high-rate digital signal by Analog Sigma-Delta block 610. The digital signal is then down-sampled and converted into a high resolution (e.g., 16-bit) and lower rate digital signal by a Digital Sigma-Delta Decimator block 620. As shown in FIG. 6, Analog Sigma-Delta block 610 generates a two-bit digital output, D_1 and D_2. **Both D_1 and D_2 are binary signals with rate R. For example, D_1 carries a sampled signal with quantization noise and D_2 carries quantization noise cancellation information.** The Digital Sigma-Delta Decimator 620 combines D_1 and D_2 and then decimates the combination by a factor M. ...
>
> FIG. 12 illustrates a low complexity, efficient polyphase structure, according to an embodiment of the present invention. **A first portion of the polyphase structure includes filters C_{11}, C_{12}, C_{13} and C_{14} for receiving inputs D_{11}, D_{12}, D_{21}, and D_{22} respectively. The outputs of filters C_{11}, C_{12}, C_{13} and C_{14} are then combined by a first summer and received by filter F_1. A second portion of the polyphase structure includes filters C_{21}, C_{22}, C_{23} and C_{24} for receiving inputs D_{11}, D_{12}, D_{21}, and D_{22} respectively. The outputs of filters C_{21}, C_{22}, C_{23} and C_{24} are then combined by a second summer and received by filter F_2.** The outputs of filters F_1 and F_2 are combined by a third summer and received by a decimator structure. The decimator structure may include a Kth order integrator filter S_1, a downsampling function block N and a Kth order differentiator S_2. The decimator structure generates a digital sigma-delta output. (Col. 17, line 13-Col. 19, line 8.) (Emphasis added by the Applicants.)

Thus, the first and second summers of Erdogan provide a sum of filtered binary signals. A sum of filtered binary digital signals is not an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors.

In distinct contrast to Erdogan, Paragraphs [0002] to [0004] and [0009] of the Applicants' published application disclose:

> [0002] There is a variety of CDMA-like transmission standards, for example UMTS, CDMA2000, TD-SCDMA, and standards for other applications based on spread spectrum technology such as the global positioning system (GPS). Each of these standards uses a variety of different codes for synchronization, spreading and de-spreading, scrambling and de-scrambling, preambles and for other purposes. These codes are typically composed from a variety of basic codes, such as pseudo noise (PN) codes, Hadamard codes and OVSF codes. The basic codes often have parameters, for example generator polynomials, offsets and masks.

[0003] A specific composite code can typically be generated by relatively simple and cheap hardware, like a linear feedback shift register (LFSR). A UMTS receiver, for example, then uses a variety of such generators to generate a specific composite code. However, this specific composite code is directly associated with the UMTS standard and therefore it is not generic.

[0004] Configurable vector processors can be equipped with code generators, so that they are capable of handling different standards and codes. Furthermore, they can be arranged to provide support for related functions such as cyclic redundancy check (CRC). A configurable vector processor would then be equipped with a plurality of generators which generate basic codes in vector format. However, a disadvantage of such a configurable vector processor is that it cannot provide a composite code which is dependent on such basic codes. This is necessary if the configurable vector processors should be flexible enough to support a variety of CDMA-like standards.

[0009] The device according to the invention is provided with at least two weighted sum units, which are able to make a selection out of a plurality of incoming basic-code vectors by means of a weighted sum operation, under the control of a configuration word. The elements of this configuration word represent the weighting factors which are used to select or deselect a basic-code vector. The selected basic-code vectors are added together and the result of the weighted sum operation is then output as an intermediate-code vector. Subsequently, the intermediate-code vectors are added together by an add unit and output as a composite-code vector. The ability to make selections out of a plurality of incoming basic-code vectors and to add intermediate-code vectors into a composite-code vector, together with the ability to configure the operations of the functional units of the device by means of configuration words, increases the flexibility of the device significantly. This flexibility is needed to support a variety of transmission standards.

Accordingly, the Applicants respectfully submit that Erdogan fails to describe, teach or suggest "at least two weighted sum units, each weighted sum unit being arranged to provide an intermediate-code vector which is a weighted sum of a plurality of the basic-code vectors" as set forth in independent Claim 1. Thus, the Applicants respectfully submit that the Office Action fails to establish a *prima facie* case of anticipation.

Independent Claim 11 recites limitations analogous to the novel limitations emphasized above in traversing the rejection of Claim 1 and, therefore, also is patentable over Erdogan. Therefore, the Applicants respectfully submit that independent Claims 1 and 11 are patentable over the cited references.

VI. CONCLUSION

As a result of the foregoing, the Applicants assert that the remaining Claims in the Application are in condition for allowance, and respectfully request an early allowance of such Claims.

If any issues arise, or if the Examiner has any suggestions for expediting allowance of this Application, the Applicants respectfully invite the Examiner to contact the undersigned at the telephone number indicated below or at ***rmccutcheon@munckcarter.com***.

The Commissioner is hereby authorized to charge any additional fees connected with this communication or credit any overpayment to Deposit Account No. 50-0208.

Respectfully submitted,

MUNCK CARTER, P.C.

Date: 12/15/2008

Robert D. McCutcheon
Registration No. 38,717

P.O. Box 802432
Dallas, Texas 75380
(972) 628-3632 (direct dial)
(972) 628-3600 (main number)
(972) 628-3616 (fax)
E-mail: *rmccutcheon@munckcarter.com*